WHITE PAPER

HFSS Regions in SIwave — Best of Both Worlds

This paper describes HFSS Regions within SIwave, a unique ANSYS SIwave technology that bolsters the accuracy of simulating signal nets with 3D discontinuities such as bondwires, vias and solderballs. This capability, which allows users to designate critical parts of a layout for full-wave 3D analysis in HFSS, helps engineers mitigate signal integrity issues in printed circuit boards (PCBs) and packages — leading to improved performance and reliability of high speed digital systems. The solution provides enhanced accuracy over traditional 2.5D solve techniques while improving speed and minimizing RAM requirements versus HFSS-only solves.

HFSS Regions in SIwave is a hybrid solution technique where HFSS' 3D electromagnetic (EM) field solver can be readily applied as part of the simulation process in tandem with the 2.5D solver in SIwave. Engineers can rely on this hybrid solver technology when extreme accuracy is required at high frequencies for critical nets in their designs.

This paper is intended to help engineers develop a solid understanding of HFSS Regions in SIwave. Aligned with this paper is a **video series** demonstrating the configuration and simulation of a PCB that utilizes this feature. To illustrate the benefits of this technology on a real-world design, we will perform simulations on a large server board with more than 40 layers as depicted in Figure 1.

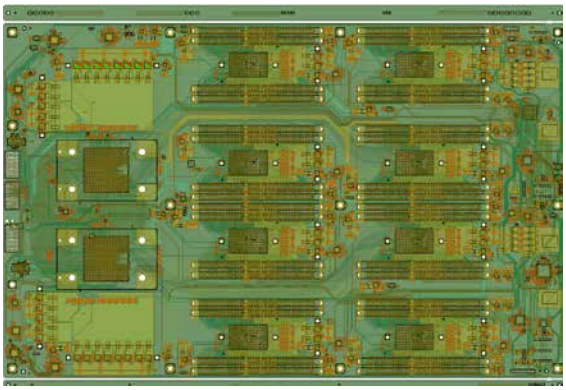


Figure 1: Server mother board

PCBs and Memory

Printed circuit boards are used in a vast array of applications spanning the automotive, aerospace, consumer electronics, networking, communications industries and others. Internet of Things (IoT) is a common theme in these industries. Numerous devices connected to the internet generate massive volumes of data that must be managed in an efficient manner. Hence, the big push for edge computing, which involves data storage and processing/computing near the source of the data (where it's generated) rather than relying solely on the cloud. Enterprises are adapting to the growing need of edge computing to manage data efficiently while also making IoT devices faster and more secure. Also, the emergence of technologies like 5G networks will require existing data centers to be upgraded. Chips, packages and PCBs of server systems must be well-designed to maintain their signal and power integrity. ANSYS simulations can mitigate signal, power and thermal integrity issues and reduce chances of failure. Well-designed chips, packages and PCBs will improve the reliability, efficiency and the overall performance of data centers.

In general, PCBs of high-end servers contain between 40 to 70 layers and thousands of signal nets. Figure 1 shows a top-down view of a server mother board's virtual prototype in ANSYS SIwave. Figure 2 displays a 3D visualization of the different layers that make up the same PCB in SIwave. This board has 43 layers, of which 20 are metal layers. It's 60 cm long and 42 cm wide. At the maximum frequency of interest (20 GHz), we are looking at an electrically large problem of 4,000 square wavelengths. There are 8 memory buffers, each controlling four dual inline memory modules (DIMMs) and each DIMM has 64 data lanes, so there are 2048 data lines.

Among the myriad of other complexities, this board has 1,547 differential pairs and two Power8 “Turismo” CPUs, which are connected to eight memory buffer modules via 9.6 Gbps differential channels. Each memory buffer module connects to four DDR3 DIMMs, for a total of 32 DDR3 DIMMs. Solving a complete ECAD design as large and complex as this PCB solely in a 3D EM field solver will be computationally expensive as signal lines typically require a very fine mesh in 3D field solvers to be modeled accurately. **Herein lies the importance of HFSS Regions within SIwave**. A hybrid 2.5D solver like SIwave can handle the size and complexity while providing fast and accurate solutions. However, at high data rates (56 Gb/s) users often rely on HFSS to increase the accuracy in critical areas such as via breakouts. HFSS Regions in SIwave is optimal for these electrically large problems since the combined solution results in a massive reduction of simulation runtime and, minimized RAM hardware requirements while providing the extreme accuracy needed for such high data rates; hence it is the **best of both worlds**.

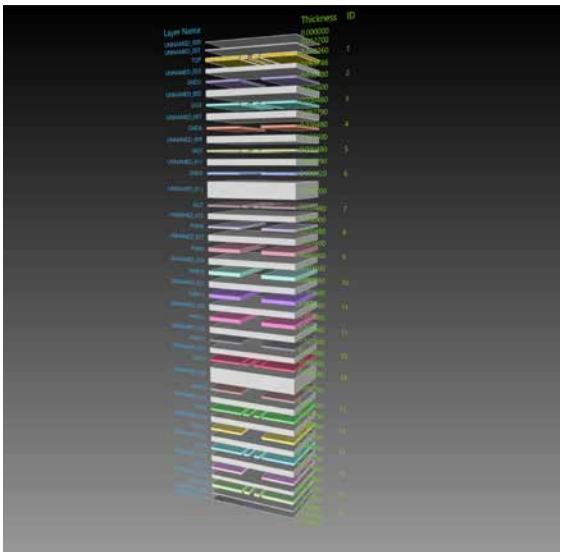


Figure 2. Layer stackup wizard (3D) in SIwave

Benefits of HFSS Regions in SIwave

ANSYS HFSS is synonymous with gold standard accuracy by virtue of its adaptive mesh refinement technique and versatile solvers for tackling 3D EM problems. Similarly, ANSYS SIwave delivers unprecedented speed, capacity and accuracy for solving electromagnetic problems involving electrical CAD (ECAD) designs. HFSS Regions in SIwave combines the power of these simulation technologies and is perfectly suited to address the extraction challenges associated with PCBs and packages. ANSYS SIwave excels in solving entire boards and packages, including long transmission lines, whereas HFSS is ideal for solving full 3D structures ranging from electrically small, medium and large sizes. From both the ANSYS SIwave user interface and the HFSS 3D Layout user interface, engineers can invoke this hybrid simulation capability to boost the accuracy of S-parameters for critical signal sets on PCBs and packages. Importantly, this increased accuracy is obtained without incurring the large computational cost of running the complete ECAD design in a full 3D EM solver. This is a powerful technique because the 3D EM field solver in HFSS and the 2.5 D solver in SIwave are applied to different parts of a PCB. For solving large and complex PCBs, a domain decomposition method such as this is a natural fit since it utilizes the strengths of two fast and accurate solvers. Thus, engineers get the best of both worlds by using this technique.

This capability in SIwave is an automated technology and obviates the need for engineers to manually create 3D models, solve them and connect them back together in a circuit tool. Electrical engineers can therefore spend less time setting up an analysis and need not be experts in 3D simulation tools to benefit from their enhanced accuracy.

Solution Technique for HFSS Regions in SIwave

HFSS Regions in SIwave is intended for areas of a board (or package) that would benefit from 3D analysis. The typical 3D objects included in an HFSS regions simulation are the connector breakout regions, via transitions, unreferenced traces, bond wires, small pad-like planes connected to selected vias and other highly 3D structures.

You need only determine the part of the PCB in SIwave you want to model using HFSS and define an extent for this region. Everything else is automatically executed in ANSYS SIwave. Figure 3 displays the HFSS regions defined on this PCB. Critical nets between Region 1 near the connector side and Region 2 near the CPU are highlighted in yellow. The connector has 192 pins and the CPU has about 2,300 pins. Table 1 lists the names of the selected nets included in the simulation.

Selected NETS
PE_SLOT2_E1_CP1_CK1_DN06
PE_SLOT2_E1_CP1_CK1_DN07
PE_SLOT2_E1_CP1_CK1_DP06
PE_SLOT2_E1_CP1_CK1_DP07

Table 1: Selected Nets

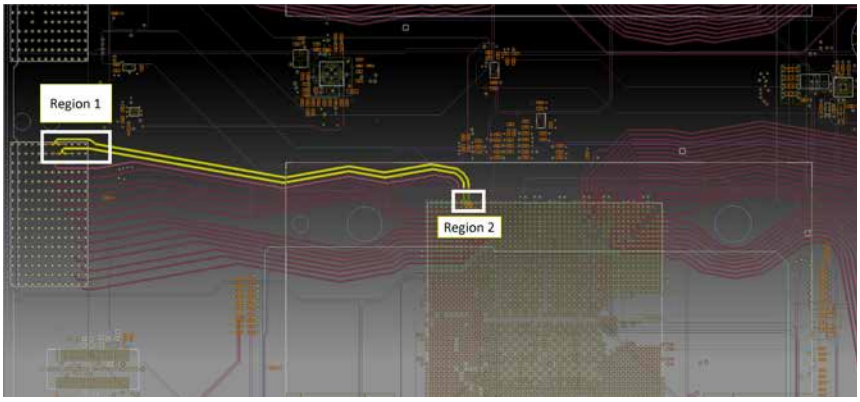


Figure 3: Top-down view of the regions defined for the PCB

The connector breakout region (1) and the BGA breakout region (2) around the CPU have a large number of tightly spaced vias as displayed by the 3D view of the defined regions in Figure 4. Therefore, the highlighted areas in Figure 3 are good candidates for modeling with HFSS Regions in SIwave — the white rectangles represent the extents drawn in SIwave. These extents can either be rectangles or polygons and are easily drawn in SIwave. You should keep the extent sizes relatively small to reduce simulation runtime. The differential signal nets connecting the vias between the connector breakout region and the vias in the breakout region near the CPU are highlighted in yellow in Figures 3 and 4. SIwave will be used to capture the interaction between the differential lines and the non-ideal power and ground planes. The 3D regions will be solved by invoking the HFSS solver from SIwave, and the S-parameter results from HFSS are back annotated to SIwave to obtain the solution of the complete board. The adaptive frequency is 10 GHz and the interpolating frequency sweep range is written in the table below.

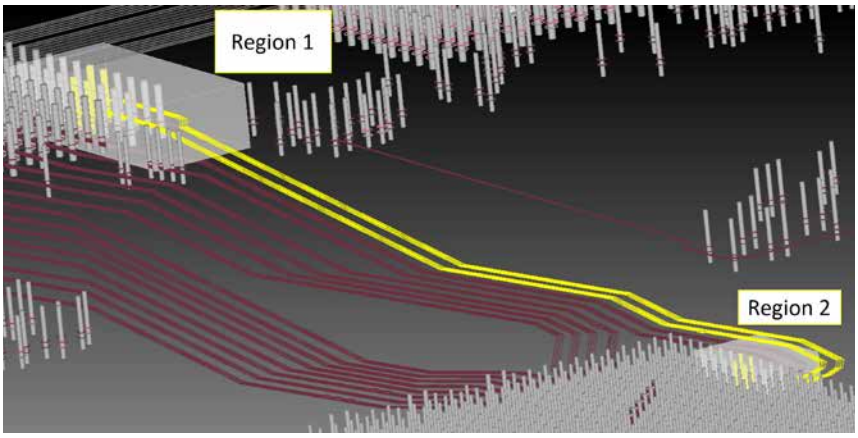


Figure 4: 3D view of the defined regions

Start Frequency	Stop Frequency	Num. Points/ Step Size	Distribution
0 Hz	0 Hz	1 Hz	Linear Step
1 Hz	100 MHz	10 Hz	by Decade
100 MHz	20 GHz	50 MHz	Linear Step

Table 2: Interpolating frequency sweep

/ Comparison of the Simulation Output in the Frequency Domain

Once the simulation is complete, the S-parameter plots can be easily exported from ANSYS SIwave to ANSYS Electronics Desktop to compare the results with and without using HFSS Regions.

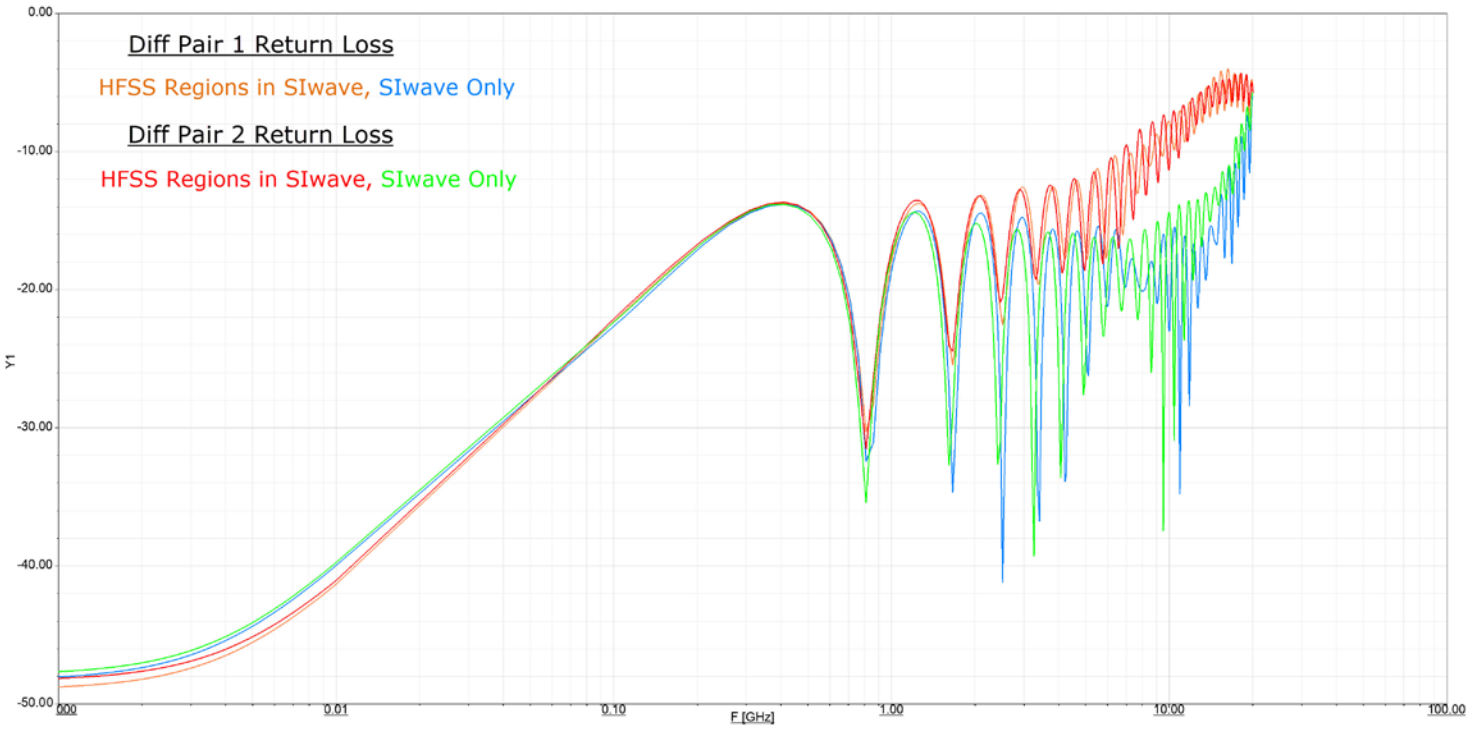


Figure 5: Return loss plot

Figure 5 shows the return loss for the differential pairs in both cases (with and without) HFSS regions. The results are similar up to about 5 GHz. Above 5 GHz, the solution with HFSS regions predicts higher return loss than the standard SIwave solution. The higher return losses are due to 3D effects in the via fields at the ends of the differential pairs. HFSS Regions in SIwave is able to capture these effects with greater accuracy than the SIwave-only solution.

Comparison of the Simulation Output in the Time Domain

To provide a thorough analysis, a comparison of the simulation output in the time domain for three cases is conducted: HFSS Regions within SIwave, SIwave-Only and Full HFSS solve of a cutout of the board containing the desired nets and the 3D regions. In order to analyze the entire signal channel with a full HFSS 3D simulation, a section of the board containing the desired nets is cut out and exported to HFSS 3D Layout. Touchstone files were exported for each of the three simulations.

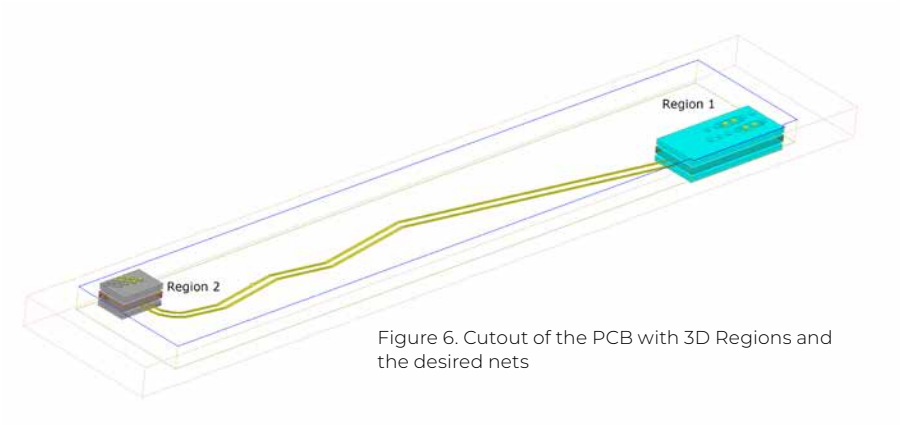
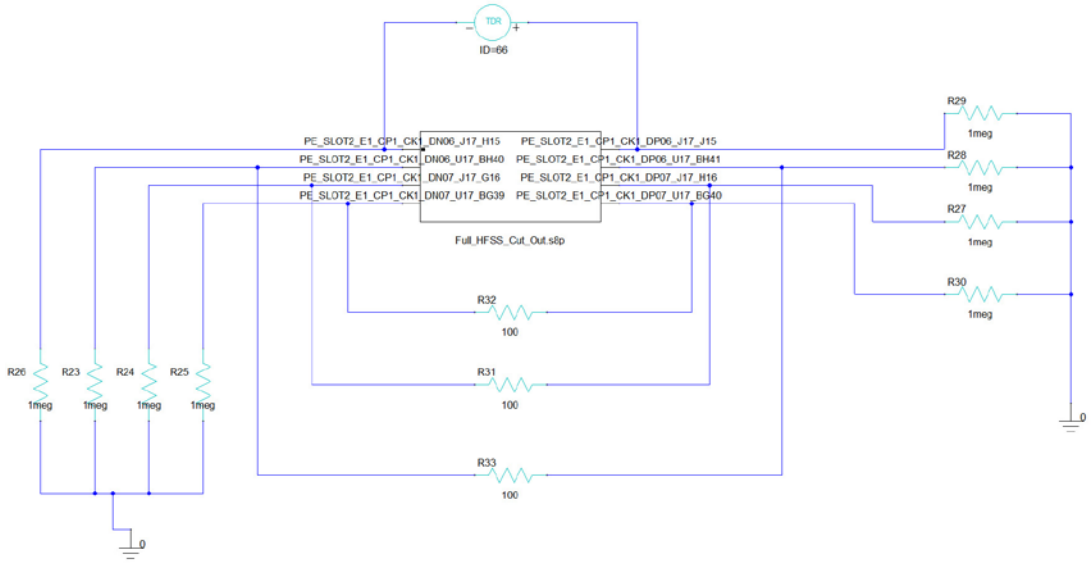


Figure 6. Cutout of the PCB with 3D Regions and the desired nets



To study the response from each of the analyses, three circuits in ANSYS Electronics Desktop were created. Each circuit contains an N-port model, which is defined by the corresponding touchstone files (*.sNp). A differential TDR component was connected to the N-port model. One of these circuits is shown in Figure 7. The TDR rise time was set to 35 ps to stress these interconnects with high speed signals.

The TDR plot showing the impedance of the signal path as a function of time and distance can be observed in Figure 8. The red curve used SIwave only. The blue curve used HFSS Regions in SIwave. The green curve shows the simulation results performed entirely in the 3D EM solver of HFSS using only a cut-out of the PCB containing the regions and the desired nets.

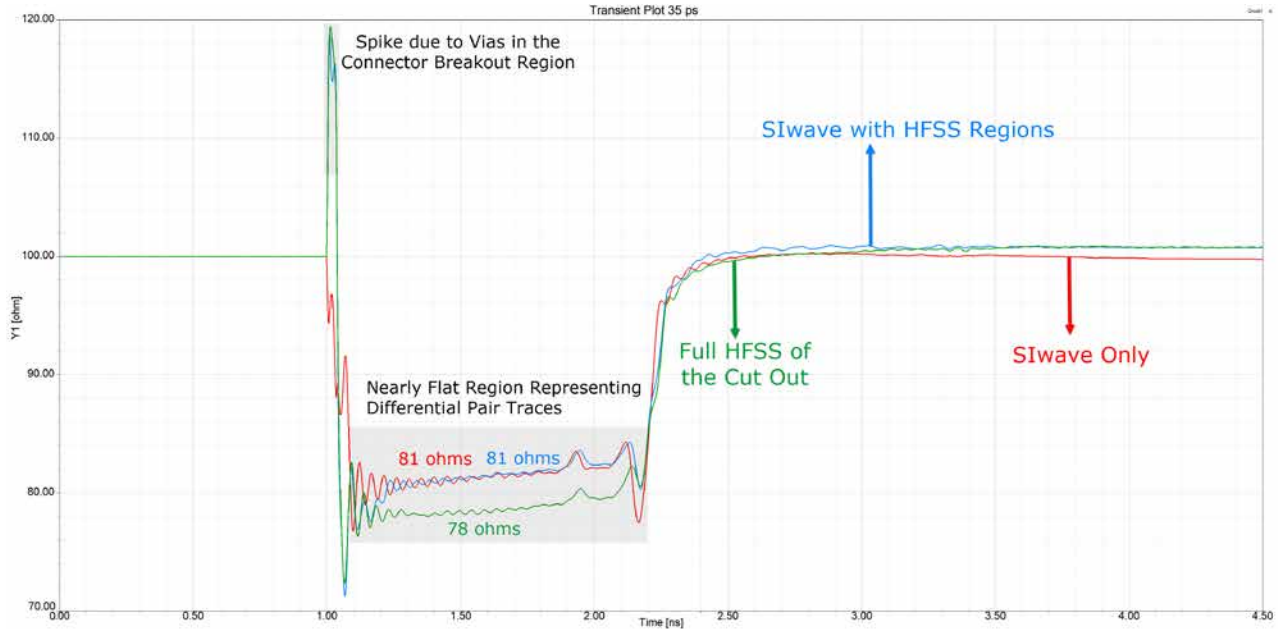


Figure 8a

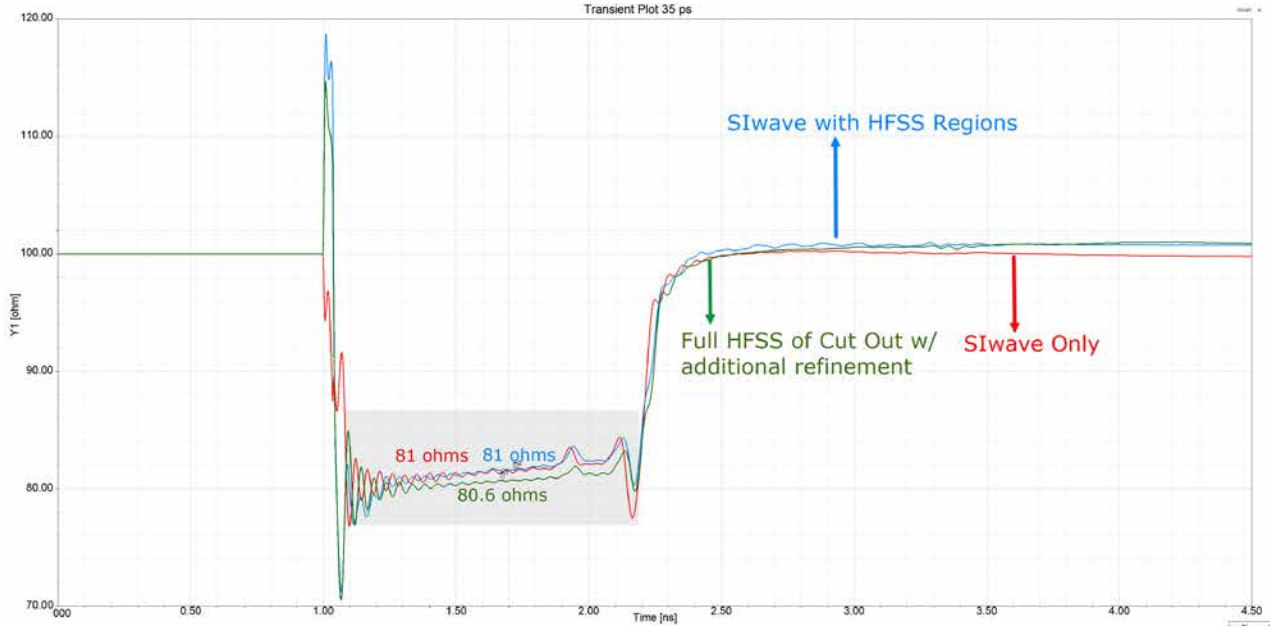


Figure 8b

Notice the nearly flat region between 1 ns to 2.2 ns representing the differential pair traces. The traces are 9 cm long, so they have a round trip delay of about 1.2 ns. The differential characteristic impedance is about 81 ohms for HFSS Regions in SIwave and SIwave-only. The results are similar between 1-2 ns except in the beginning of this time interval. The spike at the beginning is caused by the vias in the connector breakout region. The blue curve representing HFSS regions in SIwave is capturing this 3D effect here. It's picking up an inductive spike at 1 ns that SIwave-only missed. This is due to the differences in via modeling. HFSS performs a full 3D solution while SIwave uses a simplified 3D model. To verify that the HFSS solver invoked from SIwave is responsible for these differences, the results from the HFSS-only cutout simulation are superimposed as shown by the green curve in Figure 8a.

You can see that there is excellent agreement between HFSS-only and the HFSS Regions in SIwave for the inductive spike at the beginning. The full HFSS results demonstrate a slightly different differential characteristic impedance of 78 ohms instead of 81 ohms for the SIwave results. Seeding the HFSS Mesh and running more adaptive passes will better refine the mesh around the traces and produce greater accuracy in the results, hence an improved match, as shown in Figure 8b. The impedance is 80.6 ohms, a touch under 81 ohms. Simulation of long transmission line structures is more efficiently handled by the SIwave solver, whereas the simulation of 3D structures, such as vias, are better handled by the HFSS solver.

Comparison of Eye Characteristics

Finally, Figures 9A and 9B show the eye-diagram computed in SIwave with and without the HFSS regions. The results using only SIwave evidence some closing of the eye that is not present in the results using HFSS regions. Figure 9C shows the eye diagram computed for the full HFSS simulation of the cutout.

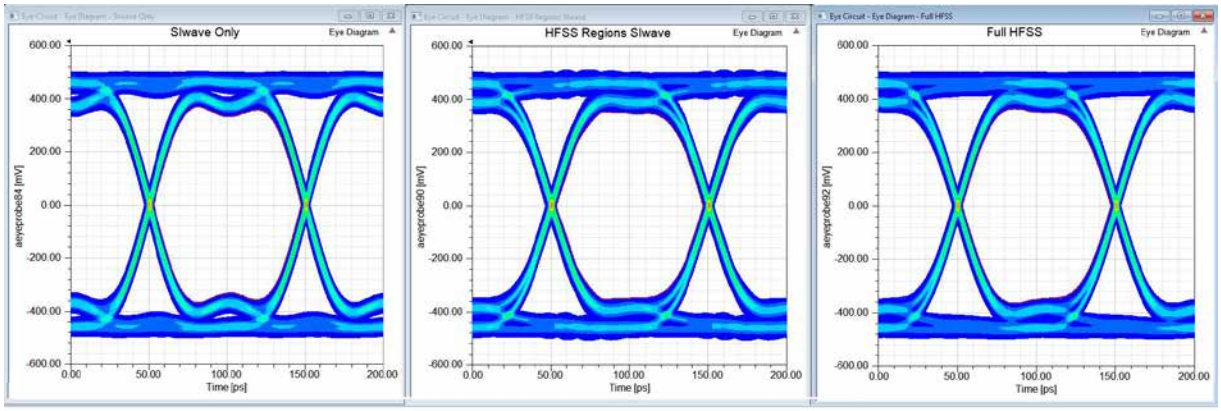


Figure 9A Figure 9B Figure 9C

Figure 9. Eye diagrams from a transient analysis at 35 ps

Eye Characteristics	SIwave Only Simulation	HFSS Regions in SIwave Simulation	Simulation of the Cutout in HFSS Only
Peak-to-Peak Jitter	6.6 ps	7.0 ps	7.0 ps
Minimum Eye Height	663.7323 mV	696.2321 mV	699.0568 mV
Minimum Eye Width	94 ps	93.6 ps	93.6 ps

Table 3: Comparison of Eye Characteristics

The eye diagram results from the HFSS Regions in SIwave simulation shows good correlation with the full HFSS simulation of the cutout. Key eye measurement metrics for the three simulations are displayed in Table 3.

The values of peak-to-peak jitter as well as the minimum eye width are identical for the HFSS Regions in SIwave and the Full HFSS simulation of the cutout. This is also true for the minimum eye width. The difference in the minimum eye height is negligible in the HFSS Regions within SIwave simulation and the full HFSS simulation of the cutout. Clearly, HFSS Regions in SIwave boosts the accuracy of the simulation.

Performance Comparison of the Three Simulations

HFSS Regions within SIwave has been shown to provide increased accuracy over the 2.5D solve techniques. The performance advantages HFSS Regions within SIwave has over the full HFSS 3D solver can be observed by comparing the computational time and memory requirements of the different simulation methods. Table 4 lists the data obtained from simulating the PCB using the three techniques. A Windows High Performance Compute (HPC) Cluster with 28 cores and 512 GB RAM was used for these comparisons.

Simulation	Time	Peak Memory Usage
SIwave Only	10 hours and 30 minutes	SIwave Solver = 67 GB
SIwave with HFSS Regions	12 hours and 25 minutes	HFSS Solver = 88 GB; SIwave Solver = 65 GB
Simulation of the Cutout in HFSS only	30 hours and 39 minutes	HFSS Solver = 55 GB

Table 4: Simulation Time and RAM for the three cases

The run time of SIwave with HFSS Regions is 16 percent more than the SIwave-standalone simulation. Sixteen percent more compute time is a relatively low price to pay and certainly rewarding in terms of obtaining increased accuracy of the critical nets on such a large and complex printed circuit board. HFSS Regions in SIwave required approximately 30 percent more peak memory usage than SIwave only — understandably so since 3D region solutions will generally require more memory than 2.5D solutions alone in SIwave. Moreover, the size of the board also is large with 40 layers. Solving the full channel cutout using HFSS only required 55 GB of memory and over 30 hours. Solving such a large board in a full-blown 3D EM solver is impractical. Using a domain decomposition approach such as HFSS Regions in SIwave is very efficient, resulting in greater accuracy.

Conclusion

Mitigating signal integrity issues in PCBs, packages and chips is of paramount importance for the proper functioning of server systems and data centers. A simulation technique such as HFSS regions in SIwave is indispensable for the analysis and design of high-speed printed circuit boards and packages and allows engineers to obtain unprecedented insight into signal integrity problems impacting their designs.

Authors
Shankar Raman, Dr. J. Eric Bracken, Manohar Raju, Dr. John Silvestro, Dr. Steven G. Pytel, Wade Smith, Howard Mark Ravenstahl.

Additional References

1. Manohar Raju, Dr. Steven G Pytel, Dr. Lawrence Williams, "Package and Board Power Integrity Design with ANSYS SIwave-PI" — White Paper.
2. Manohar Raju, Dr. J. Eric Bracken, Dr. Steven G Pytel, "Electrothermal Mechanical Stress Reference Design Flow for Printed Circuit Boards and Electronic Packages" — Technical Paper.
3. Simulation and Design of Printed Circuit Boards Utilizing Novel Embedded Capacitance Material - White Paper.
4. PCB for the analysis was used under Creative Commons ShareAlike Attribution 4.0 International (CC BY 4.0). Original board is available at: https://www.opencompute.org/wiki/Server/SpecsAndDesigns

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